EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Shreen Danamraj on February 19, 2009.

The application has been amended as follows:

Claims:

1. (Currently Amended) A system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is ~~operable~~ configured to operate with a first clock signal and said second clock domain is ~~operable~~ configured to operate with a second clock signal, said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

a first circuit portion for providing said data blocks including said header block to a second circuit portion;

control logic associated with said second circuit portion for processing said header block and generating, in response to said header block, a hint signal that gives advance notification of a possible data transfer operation, said hint signal being

~~operable~~ configured to be transferred via a synchronizer at least one data cycle prior to the transfer of said data blocks to a third circuit portion; and

a control block associated with said third circuit portion, said control block operating responsive to said hint signal to generate data transfer control signals for controlling said third circuit portion in order to control output of said data blocks in a particular ordered grouping, wherein said first circuit portion, said second circuit portion and said control logic are disposed in said first clock domain and said third circuit portion and said control block are disposed in said second clock domain.

10. (Currently Amended) A method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is ~~operable~~ configured to operate with a first clock signal (CLK1) and said second clock domain is ~~operable~~ configured to operate with a second clock signal (CLK2), comprising:

processing a header block associated with data blocks that are to be sent from said first clock domain to said second clock domain via a synchronizer;

generating a hint signal that gives advance notification of a possible data transfer operation responsive to said header block and positioning said hint signal at least one cycle prior to the location of said data blocks, said processing said header block and said generating said hint signal being performed in said first clock domain;

transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain; and

generating appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

13. (Currently Amended) A computer system having circuitry for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein said first clock domain is ~~operable~~ configured to operate with a first clock signal (CLK1) and said second clock domain is ~~operable~~ configured to operate with a second clock signal (CLK2), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M > 1, comprising:

means for processing a header block associated with said data blocks to determine whether said data blocks may be sent from said first clock domain to said second clock domain via a synchronizer;

means for generating a hint signal that gives advance notification of a possible data transfer operation responsive to said header block wherein said hint signal is ~~operable~~ configured to be positioned at least one cycle prior to the possible location of said data blocks, said means for processing a header block and said means for generating a hint signal being disposed in said first clock domain; and

means for transmitting said hint signal to a control block in said second clock domain, thereby indicating that said data blocks may be sent to receive circuitry in said second clock domain, wherein said control block generates appropriate control signals based on said hint signal for controlling output of said data blocks in a particular ordered grouping.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Sai-Ming Chan whose telephone number is (571) 270-1769. The Examiner can normally be reached on Monday-Thursday from 8:00 am to 5:00 pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

/Sai-Ming Chan/

Examiner, Art Unit 2416

March 3, 2009